JEDEC STANDARD

Semiconductor Wafer and Die Backside External Visual Inspection

JESD22-B118A

Revision of JESD22-B118, March 2011, Reaffirmed, June 2016

NOVEMBER 2021

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or call (703) 907-7559 or www.jedec.org

Published by
©JEDEC Solid State Technology Association 2021
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

This document may be downloaded free of charge; however JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

PRICE: Please refer to the current
Catalog of JEDEC Engineering Standards and Publications online at
http://www.jedec.org/Catalog/catalog.cfm

Printed in the U.S.A.
All rights reserved

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by JEDEC and may not be
reproduced without permission.

Organizations may obtain permission to reproduce a limited number of copies
through entering into a license agreement. For information, contact:

JEDEC Solid State Technology Association
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107
or call (703) 907-7559

TEST METHOD B118A

SEMICONDUCTOR WAFER AND DIE BACKSIDE EXTERNAL VISUAL INSPECTION

(From JEDEC Board Ballot JCB-21-62, formulated under the cognizance of the JC-14.1 Subcommittee on Reliability Test methods for Packaged Devices.)

1 Scope

Semiconductor wafer and die backside external visual inspection is an examination of the external non-active surface area (hereafter called backside) of processed semiconductor wafers or die. This inspection method is for product semiconductor wafers and dice prior to assembly. This test method defines the requirements to execute a standardized external visual inspection and is a non-invasive and non-destructive examination that can be used for qualification, quality monitoring, and lot acceptance. Alternate methods of inspection or techniques that provide assurance to Clause 6 elements are acceptable (e.g., functional testing, automated inspection equipment, in-line manufacturing operations, etc.).

This test method is applicable to:

- Backside inspection of semiconductor wafers and die. Wafers and die sampled for external visual inspection must be representative of final product.

This test method does not apply to or require any inspection, measurement, or analysis other than the procedure described in clause 5.0. Recommended tools and equipment for this test method are presented in clause 4.0; use of substitute tools or equipment to perform this test method is acceptable provided correlated results are obtained.

2 Terms and definitions

arc: A visual anomaly that is a curved scratch.

blemish: A visual anomaly that is an area of inconsistent finish.

burn mark: A visual anomaly with a burned appearance.

chip out: Damage resulting from a volume of material being removed by mechanical impact.

crack (in a wafer or die): A fracture within the bulk material of a wafer or die.

critical area: An area of the wafer or die for which the inspection criteria is more stringent.

NOTE The critical area should be stipulated by the appropriate drawing or specification.

dice: Plural of "die".

diced wafer: A wafer that has been separated into individual dice.