

JEDEC STANDARD

DDR5 RDIMM Standard Annex D

JESD305-R8-RCD Version 1.0

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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From JEDEC Board Ballet JCB-21-36, formulated under the cognizance of the JC-45.1 Subcommittee on registered DRAM modules, item 2273.03.

1 Scope

This standard, JESD305-R8-RCD, DDR5 Registered Dual Inline Memory Module with 8-bit ECC (EC8 RDIMM) Raw Card D Annex, defines the design detail of x8, 1 Package Rank DDR5 RDIMM with 8-bit ECC. The common feature of DDR5 RDIMM, such as the connector pinout, can be found in the JESD305, DDR5 Load Reduced (LRDIMM) and Registered Dual Inline Memory Module (RDIMM) Common Standard.

2 DDR5 Registered DIMM Design File**Table 1 — DDR5 Registered DIMM Design File**

Raw Card	Applicable Design File	Applicable BOM
D0	PC5-RDIMM_RC_D0_R100_20210611.zip	PC5-RDIMM_RC_D0_R100_20210611_BOM.xlsx
NOTE “Reference” design file updates will be released as needed. This DIMM Annex standard will reflect the most recent design files but may also be updated to reflect clarifications to the specification only. In these cases, the design files will not be updated.		

3 Module Configuration**Table 2 — Module Configuration**

SDRAM			DIMM												
Die Density	Die Organization	Pack-age Type	# of Logical Ranks ^{1,2} per PKG. Rank		# of PKG. Rank 1,2 per DIMM	# of Logical Ranks ^{1,2} per DIMM		# of SDRAM die per DIMM		Capacity per DIMM (GB)		DIMM Organization		# of Address Bits Row/Col	MO-329 Variation
			Min.	Max.		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
16Gb	2G x 8	SDP	1	1	1	1	1	10	10	16	16	2Gx80	2Gx80	16/10	AAxx
		3DS	-	-	-	-	-	-	-	-	-	-	-		
24Gb	2G x 8	SDP	1	1	1	1	1	10	10	24	24	2.4Gx80	24Gx80	17/10	AAxx
		3DS	-	-	-	-	-	-	-	-	-	-	-		

NOTE 1 When populated with single die package (SDP), package ranks per DIMM = 1.