JEDEC PUBLICATION

Recommended ESD-CDM Target Levels

JEP157A

APRIL 2022

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or call (703) 624-9230 or www.jedec.org

Published by
©JEDEC Solid State Technology Association 2022
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

PRICE: Please refer to the current
Catalog of JEDEC Engineering Standards and Publications online at
http://www.jedec.org/Catalog/catalog.cfm

PLEASE!

DON'T VIOLATE
THE
LAW!

JEDEC Solid State Technology Association
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107
or call (703) 907-7559

RECOMMEND ESD-CDM TARGET LEVELS

Foreword

CDM has become the primary real-world ESD event metric describing ESD charging and rapid discharge events in automated handling, manufacturing, and assembly of IC devices. Its importance has dramatically increased over the years as package feature sizes, capacitance, and pin count have scaled upward. In years past, arbitrary CDM protection levels had been specified as IC qualification goals with little background information available on actual/realistic CDM event levels and the protection methods available in manufacturing controls and device design for the safe production of IC components. The rapid advancement of IC technology scaling, coupled with the increased demand for high-speed circuit performance, made it increasingly difficult to guarantee a customer-specified "500 volts" CDM specification and as this update will discuss, even 250 volts can create challenges. At the same time, the required static control methods available for production area CDM protection at each process step have not been fully outlined. Therefore, a realistic CDM specification target must be defined in terms of available and commonly practiced CDM control methods and must reflect current ESD design constraints. Additionally, as technology scaling continues, very high-speed I/Os are being introduced which demand the need for lower CDM target levels in order to achieve the needed I/O performance. This is the scope of this latest update to JEP157.

By balancing improved static ESD controls specific to CDM, and limited ESD design capability in today's leading technologies, we recommend a CDM specification target level of 250 volts with consideration for lower CDM target levels in unique cases where very high-speed I/O performance is needed. These target levels are a realistic and safe CDM level for manufacturing and handling today's products using basic CDM control methods or advanced CDM control techniques as needed based on the target level.

At the same time, we show that the current trend of silicon technology scaling will continue to place further restrictions on achievable CDM levels. It is, therefore, necessary that the Industry Council presents a realistic CDM roadmap for consideration by the industry moving forward to 7 nm technologies and beyond, including 2.5D and 3D technologies.

Introduction

It is well understood in the IC industry that the charged device model (CDM) is the ESD model that best describes real-world component-level ESD events during IC manufacturing and handling. See Clause 4 for details. In contrast to HBM, where basic ESD control measures in manufacturing ensure a safe and realistic specification level (i.e. 1000 volts HBM as reported in JEP155 [1]), CDM protection requires these basic ESD controls as well as additional ESD controls such as managing against the charging of insulators, at specific process steps, to ensure safe and realistic levels for all product designs below 200 volts. Some of these additional process assessment techniques that may need to be involved are detailed out in a recently released standard practice from the ESDA entitled "Protection of Electrostatic Discharge Susceptible Items – Process Assessment Techniques", ANSI/ESD SP17.1. As IC applications have moved towards ultra-high-speed I/O interfaces (> 200 Gb/s) over the last decade, this CDM threat has been further exacerbated in terms of qualification levels to achieve design performance. This has driven the need for advanced control methods to be implemented for safe manufacturing in the production area. Combined with these new developments the sensitivity and accuracy for CDM testing have become more

critical than ever. This update to JEP157 addresses the current requirements for CDM presenting a holistic view of the CDM roadmap including both standard and advanced high-speed products.

Some important aspects of the CDM challenge must be understood:

IC Design / Development Constraints: Constraints from silicon technology scaling, IC high-speed circuit design requirements, and larger IC package size trends are impacting ESD protection capability, see Clause 5 for details. These constraints can inhibit the ESD design methodology required to meet the customer-specified 500 or 250 volt CDM levels. This is especially true for very high-speed high-performance pin design types, which have limitations in CDM discharge peak current. As a result, practical designs are restricted to 2-6 amperes of peak CDM current, which translates to a CDM target level of 125-400 volts for many advanced technology products (depending on pin-count). In the same vein, ultra-high-speed designs > 200 Gb/s in the sub-10 nm technologies can be constrained by even tighter CDM peak currents in the range of 2 to 3 amperes for non-RF I/O.

Evolution of Perceived CDM Requirements: 500 volts can no longer be routinely met for the reasons discussed above, often leading to delays in qualification and time-to-market. The more important focus should be that the designs can no longer support these previous levels and that with the available CDM control methods there is no need for higher CDM levels (≥ 500 volts) that make the designs nearly impossible to meet circuit performance. In addition, even if only a small portion of the IC products are designed to be in the market with a high-speed interface, these high-speed interfaces now require consideration for even lower CDM targets compared to most products without these interfaces. Estimates from the ESD Association's Technology Roadmap [2] do show an expected increase in the number of products that are predicted to have CDM levels below 125 volts by 2025 as shown in Figure 1.

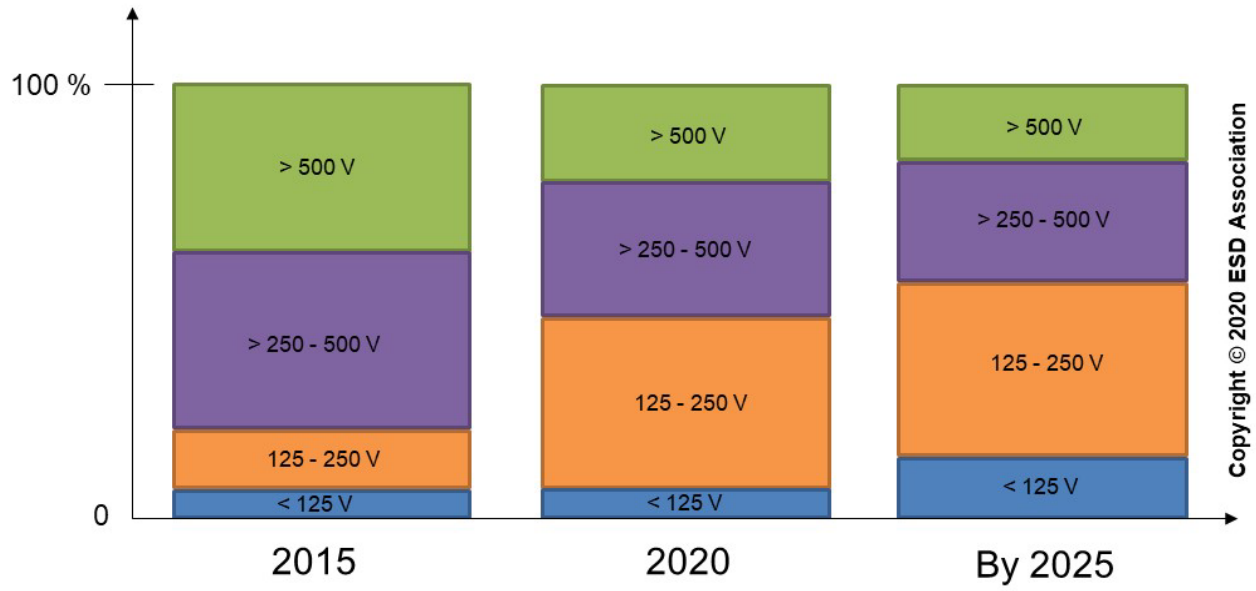

Figure 1 — Forward-Looking Charged Device Model Sensitivity Distribution Groups

Improved state-of-the-art CDM ESD control methods in practice in the industry today. Basic controls allow safe handling for devices with CDM pass voltage levels as low as 200 volts and with process assessment techniques as discussed in Clause 6 and further in ANSI/ESD SP17.1 enabling lower levels. This work has revealed several important findings that need to be considered.

A. Field return data from 11 billion IC devices show that customer returns can occur for products with CDM pass levels from 200 volts to 2000 volts, meaning control of CDM at production sites is more important than a specific performance target level. See Clause 7.
B. Field failures also can occur when proper CDM control is not established during a product ramp-up (pre-qualification), meaning that production failures must be addressed by correcting the CDM control methods at critical process steps rather than requiring the designs to pass at higher voltages than are achievable by design. See Clause 6.
C. CDM control measures are available throughout the industry to meet safe manufacturing and handling of products at 200 volts or above, meaning that products designed for CDM levels at 250 volts or 500 volts can be equally safe and reliable. Process assessment techniques as discussed in Clause 6 and further in ANSI/ESD SP17.1 can be used to address even lower CDM target levels.
D. Thus, any product with a CDM passing level of 250 volts or higher can be handled safely and reliably in a facility with basic CDM control measures. This level of protection should result in minimal impact on design and IC circuit performance requirements and make them compatible with current technology trends. See Clause 8.
E. As future IC technologies are enabled, there should be a continuous improvement of CDM control with even more advanced methods coming into practice.
F. Recently, a standard practice document ANSI/ESD SP17.1 [3] was developed by the ESD Association introducing advanced process assessment techniques valuable for assessing risks below 200V and which can be utilized for dealing with CDM at or below 125 volts. See Clause 6.

Recommended CDM Levels: Based on this extensive study, a safe and practical CDM passing level of 250 volts is recommended as outlined in Table 1 below. Products with a CDM target level lower than 250 volts should implement additional process-specific measures for CDM control, especially during product ramp-up. For products in this category, process-specific techniques, as described in ANSI/ESD SP17.1, are mandatory.

Table 1 — Recommended CDM Classification Based on Factory CDM Control

CDM classification level (tested acc. to ANSI/ESDA/JEDEC JS-002)	ESD Control Requirements
V_{CDM} ≥ 200 V	• **Basic ESD control methods** with the grounding of metallic machine parts and control of insulators according to standards like ANSI/ESD S20.20, IEC 61340-5-1, or JEDEC JESD625
V_{CDM} < 200 V	• **Basic ESD control methods** with the grounding of metallic machine parts and control of insulators + • **Process specific measures** to reduce the charging of the device **OR** to avoid a hard discharge (high resistive material in contact with the device leads) + • **Charging/discharging measurements at critical process steps following ANSI/ESD SP17.1**

Updated Roadmap for continued silicon technology scaling. With more recent developments requiring ultra-high-speed interface designs in technologies of sub-10 nm, the CDM Roadmap has been revised as shown in Figure 2. This was driven by targets for 5 nm SoCs and beyond for operations @ 56 GHz

(Nyquist) or 224 Gb/s PAM4. As designs are now limited to 75 fF of ESD loading capacitance, a target level of 125 volts has become necessary (as indicated by the red bar in the figure) for this ultra-high-speed interface. Package sizes for large ICs, such as microprocessors, at these performance levels, dictate the CDM peak discharge current. To recognize this constraint, the Industry Council is also recommending that the max target peak current of associated 224 Gb/s PAM4 high-speed IP blocks be 2.5 amperes. Advanced process assessment techniques as specified in ANSI/ESD SP17.1 can enable a path to safe manufacturing at these lower target levels. At the same time, lower performance I/Os such as standard GPIO interfaces should still be targeted at 250 volts leveraging basic control methods as described in ANSI/ESD S20.20 [4], IEC 61340-5-1 [5], and JEDEC JESD625 [6] this will help minimize the manufacturing risks on products that may have a high-performance I/O. This is explicitly shown in the figure at the 7 to 5 nm node with the green bar at 250 volts in the figure for standard I/Os, and the red bar at 125 volts for ultra-high-speed 224 Gb/s PAM4 I/O interfaces. The choice of qualification thus depends on the I/O applications.

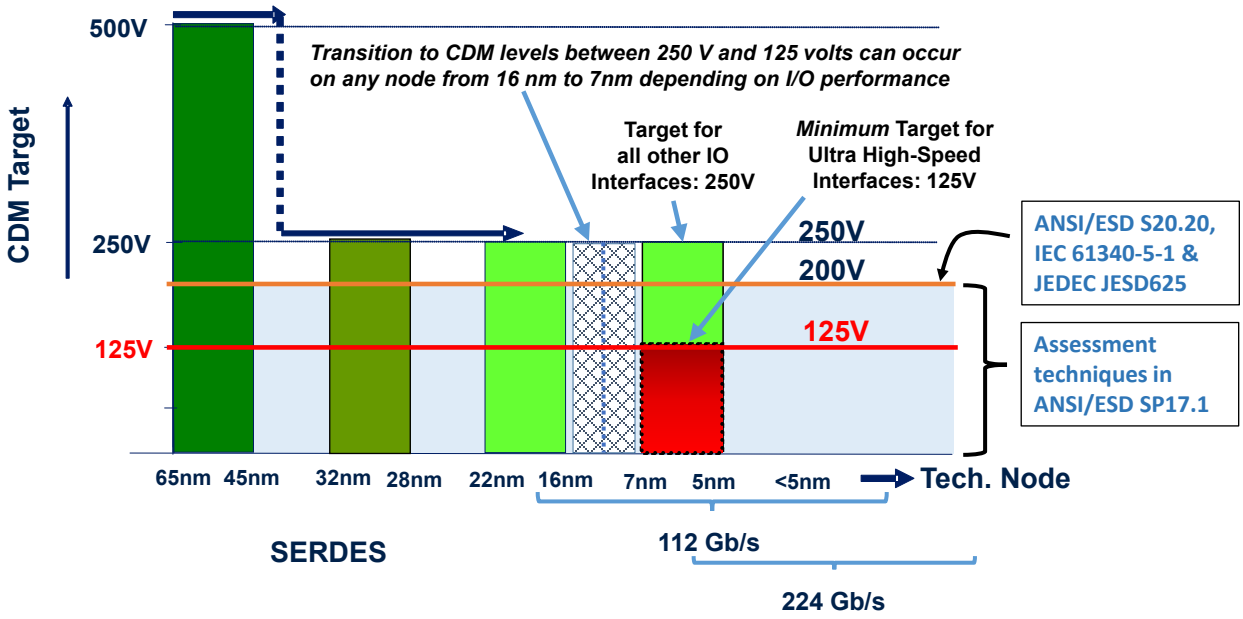

Figure 2 — Technology scaling effects on practical CDM levels and the associated CDM control requirements

As I/O performance levels increase above 56 Gb/s PAM4, a reduction in the maximum peak current design target will be needed for CDM due to reductions in the ESD design window based on technology, package size, and I/O performance. This means that even 250 volts may not be achievable and still meet performance requirements. However, care should be taken on the design side to ensure that if a target level of 250 volts cannot be met as a function of the ESD window, package size, and performance reasons, as discussed in Clause 5, that the achievable target level is *maximized* to reduce manufacturing risks. The designed target level for the product must also be in line with the manufacturing capability. Simply reducing the target level directly to 125 volts may not be prudent for the manufacturing capability. It should be noted that as CDM target levels drop below 200 volts, data, as shown in Clause 7 is limited, and proper manufacturing ESD controls may not have been implemented yet. Care should also be taken to ensure that proper ESD controls are in place and that the proper process assessments have been made in the manufacturing flow as per ANSI/ESD SP17.1 for whatever CDM target level is achievable. This will ensure the manufacturing environment can manage the risks with component target levels moving towards 125 volts.

3D IC CDM Targets: As described in the GSA roadmap [7] for 3D ICs, in 2.5D and 3D packaging processes, with die stacking some micro-bumps are not connected to the external package ball, but can experience ESD exposure during a few process steps of the manufacturing process. In these packaging technologies, the number of micro-bumps can range from hundreds up to tens of thousands, a CDM target I_{PEAK} range from 100 milliamps to 1 ampere is discussed for qualification. Careful consideration of ESD controls in a few critical process steps will guarantee the safe handling of these micro-bumps in manufacturing. The qualification can be done by assessing these internal bumps with very fast TLP (VF-TLP) or wafer-level CC-TLP equipment.

External/Internal High-Speed I/Os: Externally exposed high-speed I/Os require extra ESD control precautions in the handling, manufacturing, assembly, testing, and system installation phases. At the same time, internal I/O are not immune to ESD risks. Annex A explains how the risk of CDM events is limited with a product's internal I/O but can exist especially during printed circuit board (PCB) and system assembly if ESD control precautions are not fully implemented, while external I/O have extra precautions that may need to be taken to ensure these I/O are safe in real-world environments.

CDM Qualification of Interface IP: Determining whether an IP, when integrated into the product, is expected to pass the product's classification level is uncertain at best for the end-user. This is because the standard CDM qualification of an IP interface to a voltage class is not practical as products are qualified for a given package type or package size. For this purpose, a qualification method for IP based on a CDM peak current as a qualification parameter is suggested as guidance in Annex B.

Test Methods for Sensitive CDM Targets: As the CDM target levels are reduced to below 250 volts, proper test methods and accuracy of the test will become critical. See Annex C. Various techniques are being investigated to improve the present air discharge test method for its fidelity. At the same time, there is a much more serious effort to introduce contact-based testers for better reliability at lower CDM test voltages. It is likely a standard will be developed allowing for both air discharge and contact-based testers to be used alternatively. Currently, a method for contact based CDM testing called low-impedance contact CDM has been released as a standard practice [8]. These critical developments are concurrently taking place as CDM targets below 250 volts and as low as 125 volts are recommended.

Final Words: This revision of JEP157 addresses the critical need for CDM targets for ultra-high-speed I/O interfaces operating at data rates > 200 Gb/s and establishes that a safe level of 125 volts CDM can be recommended. At very high-speed I/O interface data rates > 56 Gb/s, a combination of factors, including the ESD design window for the technology, package size, and I/O performance can drive a reduction in the designed peak current target, meaning 250 volts may not be achievable, but design efforts should focus on maximizing the achievable peak current level to minimize manufacturing risk. Various process assessment techniques (as described in ANSI/ESD SP17.1) are necessary to address the added risks in manufacturing below 200 volts. It is important to emphasize again that all products with standard, lower performance I/Os, should still target 250 volts with manufacturing using known basic control methods such as described in ANSI/ESD S20.20, IEC 61340-5-1, and JEDEC JESD625. Better I_{PEAK} control for accuracy at lower voltages in the CDM standard test methods to validate these CDM target levels is in progress. Although not previously considered for any packaged product, interface IP qualification needs to be addressed and this can be achieved by using a recommended standard for peak current as the target. Finally, it is also recognized that exposed high-speed interface I/Os in a system need special ESD protection requirements, whether they are considered external to the system or not.

RECOMMEND ESD-CDM TARGET LEVELS

Contents

RECOMMEND ESD-CDM TARGET LEVELS

(From JEDEC Board Ballot, JCB-22-02, formulated under the cognizance of the JC-14.3 Subcommittee on Silicon Devices reliability Qualification and Monitoring.)

1 Scope

The intent of this report is to document and provide critical information to assess and make decisions on safe CDM ESD level requirements. The scope of this document is to provide this information to quality organizations in both semiconductor companies and their IC customers.

Special Notes on System Level ESD:

1. This work and the recommendations therein are intended for component level safe ESD requirements and will have little or no effect on system level ESD results.

2. Systems and System boards should continue to be designed to meet appropriate ESD threats regardless of the components in the systems that are meeting the new recommendations from this work, and that all proper system reliability must be assessed through the IEC test method.

2 References

[1] JEDEC JEP155B: "Recommended ESD Target Level for HBM Qualification," July 2018, http://www.jedec.org.

[2] ESD Technology Roadmap from the ESD Association, https://www.esda.org/standards/

[3] ANSI/ESD SP17.1-2020 "For the Protection of Electrostatic Discharge Susceptible Items – Process Assessment Techniques", 2020 http://www.esda.org/standards/esda-documents.

[4] ANSI/ESD S20.20-2014, "Development of an Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment", July 2014 http://www.esda.org/standards/esda-documents.

[5] IEC 61340-5-1:2016, "Protection of Electronic Devices from Electrostatic Phenomena – General Requirements", May 2016 http://webstore.iec.ch

[6] JEDEC JESD625B "Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices", January 2012 http://www.jedec.org.

[7] Global Semiconductor Alliance, "Electrostatic Discharge (ESD) in 3D-IC Packages", Version 1.0, January 2015 http://www.gsaglobal.org/working-groups/3d-ic-packaging/.

[8] ANSI/ESD, SP5.3.3-2018. "Low Impedance Contact CDM as an Alternative CDM Characterization Method", February 2019.

[9] T.S. Speakman, "A Model for the Failure of Bipolar Silicon Integrated Circuits Subjected to Electrostatic Discharge", International Reliability Physics Symposium (IRPS), pp. 60-69, 1974.

[10] P. R. Bossard, R. G. Chemelli and B. A. Unger, "ESD Damage from Triboelectrically Charged Pins," EOS/ESD Symposium 1980.

[11] R. Renninger, M-C. Jon, D.L. Lin, T. Diep, and T.L. Welsher, "A Field-Induced Charged-Device Model Simulator", EOS/ESD Symposium pp. 59-71, 1989.

[12] R. Renninger, "Mechanisms of Charged-Device Electrostatic Discharges", EOS/ESD Symposium Pp. 127-143, 1991.