JEDEC
STANDARD

DDR5 RDIMM Standard Annex B

JESD305-R4-RCB
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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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From JEDEC Board Ballet JCB-21-34, formulated under the cognizance of the JC-45.1 Subcommittee on registered DRAM modules, item 2273.14.

1 Scope

This standard, JESD305-R4-RCB, DDR5 Registered Dual Inline Memory Module with 4-bit ECC (EC4 RDIMM) Raw Card B Annex, defines the design detail of x4, 2 Package Ranks DDR5 RDIMM with 4-bit ECC. The common feature of DDR5 RDIMM, such as the connector pinout, can be found in the JESD305, DDR5 Load Reduced (LRDIMM) and Registered Dual Inline Memory Module (RDIMM) Common Standard.

2 DDR5 Registered DIMM Design File

Table 1 — DDR5 Registered DIMM Design File

Raw Card	Applicable Design File	Applicable BOM
B0	PC5-RDIMM_RC_B0_R100_20210622.brd	PC5-RDIMM_RC_B0_R100_20210622_BOM.xlsx

NOTE 1 "Reference" design file updates will be released as needed. This DIMM standard will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only. In these cases the design files will not be updated.

3 Module Configuration

Table 2 — Module Configuration

SDRAM					DIMM										
Die Density	Die Organi-zation	Pack-age Type	# of Logical Ranks [1,2] per PKG. Rank		# of PKG. Rank 1,2 per DIMM	# of Logical Ranks [1,2] per DIMM		# of SDRAM Die per DIMM		Capacity per DIMM (GB)		DIMM organization		# of Address Bits Row/Col	MO-329 Variation
			Min.	Max.		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
16 Gb	4G x 4	SDP	1	1	2	2	2	36	36	64	64			16/11	AAxx
		3DS	2	8	2	4	16	72	288	128	512	16Gx72	64Gx72		

NOTE 1 When populated with single die package (SDP), package ranks per DIMM = 2.
NOTE 2 When populated with single load stacked packages (3DS), logical ranks per package rank = 2-8. Logical ranks per DIMM = 4-16.